A 0.64-pJ/Bit 28-Gb/s/Pin High-Linearity Single-Ended PAM-4 Transmitter With an Impedance-Matched Driver and Three-Point ZQ Calibration for Memory Interface

Yong-Un Jeong, Member, IEEE, Hyunkyu Park, Changho Hyun, Joo-Hyung Chae, Member, IEEE, Shin-Hyun Jeong, and Suhwan Kim, Senior Member, IEEE

Abstract—A single-ended four-level pulse-amplitude modulation (PAM-4) transmitter (TX) for memory interfaces achieves high signal integrity by combining an impedance-matched PAM-4 driver with a three-point ZQ calibration scheme. This improves PAM-4 linearity by allowing the driver to compensate for its impedance variation caused by the change in the drain-source voltage \( V_{DS} \) to suit the four output levels considering both the TX and the receiver (RX). Resistors and inductors are eliminated from the voltage-mode (VM) driver, reducing the area requirement. The two-tap asymmetric feed-forward equalization (FFE) allocates six different coefficients to each minimum pull-up and pull-down transition, compensating for nonlinear equalization strengths and asymmetric characteristics of the driver. A prototype chip fabricated in the 65-nm CMOS has an area of 0.0333 mm\(^2\) and consumes 0.64 pJ/bit. It achieves a data rate of 28 Gb/s/pin with a ratio level separation mismatch (RLM) of 0.993.

Index Terms—Four-level pulse-amplitude modulation (PAM-4) transmitter (TX), memory interface, single-ended signaling, voltage-mode (VM) driver, ZQ calibration.

I. INTRODUCTION

DYNAMIC random access memory (DRAM) is used in an increasingly wide variety of applications. Different types of DRAM have been developed for different applications. Double data rate (DDR) DRAM is used for general applications [1], while low-power DDR (LPDDR) DRAM offers reduced power consumption for mobile devices [2].

Graphics DDR (GDDR) DRAM favors higher bandwidth over capacity [3], and high-bandwidth memory (HBM) provides even higher bandwidth by stacking dies using through-silicon via (TSV) [4]. Despite this specialization, all DRAMs are designed to have the highest bandwidth and the lowest power consumption, compatible with the cost of production.

Modern DRAM interfaces, with a large number of I/O pins, use single-ended non-return-to-zero (NRZ) signaling for high pin efficiency and cost-efficiency [1]–[4]. Through many generations of DRAM, the data rates per pin have been raised by increasing the clock frequency. However, DRAM process with low performance has a limitation in increasing the clock frequency of the internal circuit [5]. Narrowing the unit interval (UI) makes the signals more vulnerable to frequency-dependent channel loss. While additional circuits can compensate for these performance issues, increasing frequency requires extra power consumption. These side effects lead to saturation of the bandwidth improvement through frequency increase in NRZ signaling [6].

To overcome the limited data rate of NRZ signaling, multilevel signaling has been attempted to be applied to memory interfaces. The schemes which have been proposed include duobinary [7], C-PHY [8], three-level pulse-amplitude modulation (PAM-3) [6], and four-level PAM (PAM-4) [5], [9] signaling. In PAM-4, a symbol is freighted with 2-bit information by means of amplitude modulation of the signal. This scheme, which has been proven in other applications of high-bandwidth signaling [10]–[15], is advantageous in applications with high-frequency attenuation because a PAM-4 signal has twice the UI of the NRZ signal of the same data rate, as well as high spectral efficiency [10]. PAM-4 doubles the bandwidth while maintaining the frequency of on-chip circuits, such as clock generators, clock distributors, serializers, and data buffers. Therefore, PAM-4 is an attractive solution for next-generation memory interfaces, where the DRAM side uses a lower performance technology.

In this article, we present a low-power, high-linearity single-ended PAM-4 transmitter (TX) for memory interfaces [16]. A voltage-mode (VM) driver is combined with an auxiliary pull-up (PU) driver to achieve both impedance matching and high linearity. This TX only requires a small...
II. CONVENTIONAL PAM-4 TXS

While PAM4 allows for reduced frequencies, a signal divided into four voltage levels has a reduced voltage margin equal to one-third of that of an NRZ signal with the same total amplitude. The three voltage increments in a PAM-4 signal have vertically reduced eyes, which are sensitive to noise such as inter-symbol interference (ISI), crosstalk, and reflection, resulting in a low signal-to-noise ratio (SNR) [11]. Since the smallest eye determines the overall performance, PAM-4 requires its four voltage levels to have high linearity, thus ensuring high signal integrity.

A current-mode (CM) driver with stable current sources, such as the current-mode logic (CML) driver [10], [11] shown in Fig. 1(a), or the low-voltage differential signaling (LVDS) driver [12] shown in Fig. 1(b), has a highly linear output. However, a CM driver theoretically consumes two to four times more current than a VM driver and requires a higher supply voltage and greater area for a stable current source. A CM driver is problematic because differential signaling is not suitable for memory applications, which use single-ended signaling for pin efficiency.

A PAM-4 VM driver is more susceptible to nonlinearity because the impedance variation in PU and pull-down (PD) drivers caused by the changes in output level results in signal levels with poor linearity, as well as mismatched impedance with the channel. Previous PAM-4 VM drivers incorporate passive resistors, which are more tolerant to impedance variation, in series with each MOSFET to reduce impedance variation, as shown in Fig. 1(c) and (d) [13]–[15]. The output impedance of the TX is then determined by the sum of the impedance of the MOSFET and the passive resistor. Therefore, the larger the impedance of the passive resistor compared with that of the MOSFET, the smaller the variation in the output impedance.

Recent memory interfaces use a low-voltage swing terminated logic (LVSTL) driver, also referred to as an N-over-N driver or an NMOS-only single-ended VM driver, to reduce...
area for NRZ signaling, as shown in Fig. 2(a) [18]–[20]. The small driver allows the pre-driver to have a small size, low power consumption, and simultaneous switching noise (SSN), as well as an enhanced bandwidth by reducing the capacitive power consumption, and simultaneous switching noise (SSN), as shown in Fig. 2(a) [18]–[20]. The driver for PAM-4 signaling.

Fig. 2. (a) LVSTL driver for NRZ signaling [18]–[20] and (b) LVSTL-based driver for PAM-4 signaling.

Like an LVSTL driver, this NMOS PU driver operates in the linear region and so the variation in current from the changes in the source voltage can be expressed as follows [19]:

\[
I_{PU} = \frac{1}{2} \beta (2(V_{DD} - V_{TH})(V_{DDQ} - V_{OUT}) + (V_{DDQ} - V_{OUT})^2)
\]

where \( \beta \) is \( \mu_n \cdot C_{OX} \cdot (W/L) \), in which \( \mu_n \) is the electron mobility and \( C_{OX} \) is the gate oxide capacitance per unit area, and \( V_{TH} \) is the threshold voltage. \( V_{DD} \) is the supply voltage for the memory core including the pre-driver, \( V_{DDQ} \) is the supply voltage for the driver and is lower than \( V_{DD} \) to reduce power consumption. When the NMOS constitutes the PD driver, the gate voltage is high, but the drain voltage, which is its output, is low. Thus, the PD drivers also operate in the linear region and the change in current with drain voltage can be expressed as follows:

\[
I_{PD} = \frac{1}{2} \beta [2(V_{DD} - V_{TH})V_{OUT} + V_{OUT}^2].
\]

From (1) and (2), the LVSTL-based driver has asymmetric current characteristics due to the PU and PD drivers [17] and its impedance will change with the output voltage. Note that memory interfaces that use bidirectional signaling have an RX termination consisting of a passive series resistor and a MOSFET. The passive series resistor may be omitted, but the MOSFET is required to allow ON/OFF operation. Therefore, the smallest RX termination is realized as MOSFET-only structure. Such an RX termination, like a PD driver, will operate in the linear region and will also have a variable impedance.

The variation in the impedance of the PU and PD drivers can cause output levels to fluctuate, resulting in degraded signal integrity, which is particularly significant for PAM-4. Fig. 3 shows how an LVSTL-based PAM-4 driver generates its four output levels. The operation assumes that all PU and PD drivers are calibrated to have the correct impedance at only the highest signal level, which is \( V_{DDQ}/2 \), for the same voltage swing as the NRZ signal. At the two intermediate levels, “+2 level” and “+1 level,” which, respectively, correspond to the inputs of “10” and “01,” the PU and PD drivers do not provide the correct impedances and output levels. The output impedance of the PAM-4 driver at each output level must be matched to the channel, which can be expressed as follows:

\[
R_{PU,Total} \parallel R_{PD,Total} = Z_0 \quad (3)
\]

where \( R_{PU,Total} \) and \( R_{PD,Total} \) are, respectively, the total impedances of the turned-on PU drivers and PD drivers, and \( Z_0 \) is the characteristic impedance of the channel. The output level of this driver can be expressed as

\[
V_{OUT} = \frac{R_{PD,Total}}{R_{PU,Total} + R_{PD,Total}} \parallel R_{RX} \cdot V_{DDQ}. \quad (4)
\]

For a linear output, the driver must have the following output levels with equal intervals: \( V_{DDQ}/2 \), \( V_{DDQ}/3 \), \( V_{DDQ}/6 \), and \( V_{SSQ} \). Because the impedance of the PU and PD drivers changes with the output voltage, in particular at the two intermediate levels, this driver is structurally unable to satisfy the impedance matching and linearity conditions required for PAM-4.

III. PROPOSED PAM-4 TX

Fig. 4 shows the overall architecture of the proposed TX. A 32-bit data from a pseudorandom-bit-sequence (PRBS) generator are multiplexed in a 32:8 serializer and transmitted
A. High-Linearity and Impedance-Matched PAM-4 Driver

To achieve both high linearity and impedance matching, we introduce a new PAM-4 driver with three PU drivers and two PD drivers, as shown in Fig. 5(a). This driver has a resistorless architecture, which offers the advantages as an LVSTL driver for NRZ signaling, and the LVSTL-based PAM-4 driver, which we have just described.

Fig. 5(b) shows how this driver generates four signal levels for PAM-4, which are determined by the impedances of the turned-on PU and PD drivers and RX termination as in (4). The additional PU driver allows for a different number of PU drivers to be turned on at each signal level so that at least one PU driver can provide the correct impedance at any given level. The PU NMOS M\text{PU0} is calibrated to have the correct impedance at “+1 level,” but it has an incorrect impedance at other levels since the impedance changes with the drain–source voltage (V\text{DS}) as in (1). At “+2 level,” the error in the impedance of M\text{PU0} is corrected by calibrating M\text{PU1}. At the “+3 level,” the combined impedance error of M\text{PU0} and M\text{PU1} is corrected by calibrating M\text{PU2}. PD drivers are compensated by calibration similarly. Therefore, the proposed PAM-4 driver with an additional PU driver has correct impedance for all signal levels. For impedance matching and linearity, the correct impedances of PU drivers and PD drivers turned on at each level are derived through (3) and (4), which are summarized in Table I. Note that these calculations also accommodate variation in the RX termination. The parallel impedance value of the PU and PD drivers turned on at each level is Z\text{0} for the driver to have a constant output impedance as in (3), while the desired output levels are obtained with RX termination as in (4). For example, at “+2 level” the turned-on PU drivers are M\text{PU0} and M\text{PU1}, and the turned-on PD driver is M\text{PD1}. The output impedance of the TX at this level is the parallel impedance of these drivers, R\text{PU0} || R\text{PU1} || R\text{PD1} or Z\text{0}. The output level determined by (4), R\text{PD1} || R\text{RX}/(R\text{PU0} || R\text{PU1} + R\text{PD1} || R\text{RX}) · V\text{DDQ}, is equal to V\text{DDQ}/3.

Since the total impedance of all the PU drivers at “+3 level” is Z\text{0}, the total size of the PU drivers is the same as an equivalent LVSTL driver for NRZ signaling and is much less than that of a VM PAM-4 driver using series resistors. The small driver size, similar to that of the LVSTL driver, provides low SSN, low power requirement, and high bandwidth. The proposed driver also offers lower switching noise between “+2 level” and “+1 level.” The previous VM PAM-4 driver requires switching both PU drivers and PD drivers to make this transition, whereas the proposed driver shares a PU driver and a PD driver between these levels.

Fig. 6 shows the circuit implementation of our PAM-4 driver. Each PU and PD driver is segmented into a 5-bit binary structure for independent impedance control. The impedance of each PU and PD driver is precisely adjusted in the ZQ calibration procedure described in Section IV.

B. Low-Power Mode of PAM-4 Driver

At lower data rates, the UI of the signal is longer, and thus, the requirements are generally more relaxed. Impedance at either the TX or RX is likely to be better matched, and

<table>
<thead>
<tr>
<th>Output level</th>
<th>Turned-on devices</th>
<th>Impedance</th>
<th>Z\text{OUT}</th>
</tr>
</thead>
<tbody>
<tr>
<td>V\text{DDQ}/2</td>
<td>M\text{PU0}</td>
<td></td>
<td>M\text{PU1}</td>
</tr>
<tr>
<td>V\text{DDQ}/3</td>
<td>M\text{PU0}</td>
<td></td>
<td>M\text{PU1}</td>
</tr>
<tr>
<td>V\text{DDQ}/6</td>
<td>M\text{PU0}</td>
<td></td>
<td>M\text{PD1}</td>
</tr>
</tbody>
</table>

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Fig. 6. Circuit implementation of the proposed PAM-4 driver.

Fig. 7. Operation of the proposed PAM-4 driver in the low-power mode.

The impedance may be subject to fewer discontinuities. This reduces the need for impedance matching at the other end of the channel [21]. For example, DRAM interface needs low-power operation mode. In this mode, impedance matching requirements are relatively relaxed compared with normal operation [22].

The proposed PAM-4 driver offers a low-power mode to operate in accordance with the low-power mode of a DRAM, in which a lower power requirement is achieved by reducing impedance matching on the TX side while maintaining output linearity. Fig. 7 shows how our PAM-4 driver operates in the low-power mode. The driver uses only its PU drivers, in a configuration similar to a pseudo-open drain (POD), to eliminate short current paths, while the additional PU driver compensates for impedance variation to produce a linear output. For output linearity, the correct impedance of each PU driver is derived through (3), which is summarized in Table II. These impedances are correctly adjusted by the same ZQ calibration scheme for normal operation, and therefore, additional calibration is not required for low-power operation. The total impedance of the three PU drivers is \( Z_0 \) at \( V_{DDQ/2} \), which is the same value as that of normal operation, eliminating the need for larger driver size in the low-power mode. In the low-power mode, the power consumed at the intermediate levels is reduced and depends on the impedance of the RX termination. If the variation in the RX termination is zero, the total power consumption of the driver is reduced by about 22.2% compared with that in normal operation.

C. PAM-4 Encoder

Our PAM-4 driver unlike previous PAM-4 drivers has three PU drivers and two PD drivers. Since MSB and LSB signals are not used, a separate encoder is required. The relationship between the signals for our driver and MSB and LSB signals can be derived from the driver operation presented in Fig. 5(b), resulting in the encoder structure and encoding logic shown in Fig. 8. The single-stage encoder is implemented with simple logic gates and adds little complexity to the system. Because the encoder is located in front of the final 4:1 serializers, it can operate at low speed and the jitter that it generates is compensated by the sampling clock in the 4:1 serializer, as shown in Fig. 8.

D. Two-Tap Asymmetric FFE

The strength of equalization depends on the current added during the transition of the output signal and changes with the output level. Previous PAM-4 VM driver applies equalization according to the change in MSB and LSB [13]–[15]. However, since this does not consider the output level, equalization of different strengths is applied according to the location of the transition even for the equally sized transitions. In addition, the LVSTL structure requires different equalization strengths for the PU and PD drivers due to their asymmetric characteristics [17]. Fig. 9(a) shows the structure of the two-tap asymmetric FFE driver in the proposed TX. The three PU and three PD drivers provide six different equalization coefficients, which are responsible for six minimum PU and PD transitions for four output levels, as shown in Fig. 9(b). Applying equalization based on minimum transitions instead of MSB and LSB allows the FFE coefficients to be independently adjusted according to the location of each transition, which compensates for the nonlinearity of equalization strength. The FFE driver also provides different FFE strengths for the PU
and PD drivers to compensate for asymmetric characteristics of an NMOS-only structure. Each PU and PD driver of the FFE driver is designed to support an FFE coefficient of up to 6 dB in terms of driver size. During actual operation, this value is smaller because the ratio of voltage swing to size becomes smaller for high output swing.

Pulse-based pre-emphasis is enabled during each data transition, which tunes the impedance of the driver to match the channel. However, the output impedance of the VM driver is matched in a section in which the output voltage is kept constant and is changed during transition. Pre-emphasis increases the slew rate during transition, so that the voltage at which the impedance is matched can be reached more quickly [23].

IV. THREE-POINT ZQ CALIBRATION FOR PAM-4

The output impedance of the VM driver plays an important role in preventing signal reflection through impedance matching with the channel and determining the amplitude of the output signal, both of which are critical at high data rates. Memory interfaces typically use a ZQ calibration circuit to set the correct output impedance for NRZ signaling [2], [3] by comparing the impedance of the driver with the external reference resistor through the ZQ pin. In the case of PAM-4 signaling, which uses four voltage levels, a correct output impedance is of even greater importance because an incorrect impedance directly reduces the output linearity, making the intervals between the levels unequal. Impedance control loops can be used in a PAM-4 driver [13], [14], but the one-point impedance control cannot compensate for impedance variation due to the changes in $V_{DS}$ of the MOSFETs in the driver and may produce an incorrect output impedance at output levels other than the control point.

Fig. 10 shows the proposed ZQ calibration scheme for PAM-4 signaling. The calibration consists of a block similar to the ZQ calibration with a replica driver and an external reference resistor for NRZ signaling and a block connected to the DQ driver. From (4), the output amplitude is determined not only by the PU and PD drivers but also by the impedance of the RX termination. The DQ driver is connected to the RX termination through the output DQ pin. Therefore, the block with the replica driver can obtain exact resistance information required via the external reference resistor for impedance matching, while the block with the DQ driver can obtain variation information on the RX through the DQ pin to achieve the correct output levels. Placing comparators and counters at each DQ pin requires large area in a DRAM with a large number of DQ pins. However, high linearity can only be achieved if the variation in the RX termination is detected. Solutions considering a tradeoff between area and linearity include using a single representative calibration for a certain number of DQ pins and sharing one calibration circuit between several DQ pins.

The ZQ calibration scheme for PAM-4 has calibration points at $V_{DDQ/2}$, $V_{DDQ/3}$, and $V_{DDQ/6}$ corresponding to the three signal levels. This allows accurate calibration of the impedance of the PU and PD drivers at each level of PAM-4, as shown in Table I. Fig. 11 shows how the two loops operate at one calibration point, $V_{DDQ/6}$. As shown in Fig. 11(a), the block with the DQ driver in the first loop finds the strength of the PU driver until the output voltage, which is determined by the impedance ratio of the PU driver and the RX termination, is equal to the reference voltage of $V_{DDQ/6}$. After calibration, the code in the counter is set to C0. The other block, which contains the external resistor, also controls the PU driver so that the output voltage is equal to $V_{DDQ/6}$, and the code stored in the counter is set to C1. C0 and C1 contain information on the variation in the RX termination and impedance information on the PU driver at the target level, respectively. The impedance of the PU driver PU0, which is turned on at $V_{DDQ/6}$, can be calculated through these results and can be expressed as follows:

$$R_{PU0} = 6[Z_0 \| (Z_0 - \Delta_1)] = \frac{6}{5}(R_{CO} \| R_{C1}) = R_{5/6(C0+C1)}. \tag{5}$$

From (5), the ZQ code for PU0, which is $C_{PU0}$, is determined to be $5/6 \cdot (C0 + C1)$.

Fig. 11(b) shows the operation of the second loop, during which only the block containing the DQ driver operates. The
PD driver is adjusted so that the voltage at the output node reaches the target level while the ZQ code, $C_{PU0}$, obtained from the first loop is applied to the PU driver. The ZQ code obtained by this loop, $C_2$, corresponds to the total impedance of the PD drivers, PD0 and PD1, which are turned on at $V_{DDQ}/6$.

The identical procedure is used at the second calibration point, $V_{DDQ}/3$. The codes obtained from the first loop are $C_3$ and $C_4$, which, respectively, contain variation information of the RX termination and impedance information of the PU driver at $V_{DDQ}/3$. The total impedance of PU0 and PU1, which are turned on at the target level $V_{DDQ}/3$, can be calculated through $C_3$ and $C_4$, which can be expressed as follows:

$$R_{PU0} \parallel R_{PU1} = \frac{3}{2} \frac{Z_0 \parallel (Z_0 - \Delta_0)}{R_{C3} \parallel R_{C4}} = R_{2/3} (C_3 + C_4).$$

The second loop adjusts the strength of the PD driver so that the voltage at the output node is $V_{DDQ}/3$, while the code $2/3 \cdot (C_3 + C_4)$ is supplied to the PU driver. The result, $C_5$, becomes the ZQ code for PD1.

At the third calibration point of $V_{DDQ}/2$, the first loop can run in either of the blocks, since we assume that the RX termination is calibrated at the highest level. The ZQ code $C_6$ has the strength information on the total impedance of all the PU drivers.

Table III summarizes the ZQ codes determined at the three calibration points. These codes are then supplied to the drivers and change their strengths to simultaneously provide matched impedances and equally spaced signal levels.

**Table III**

<table>
<thead>
<tr>
<th>Device</th>
<th>Normal operation</th>
<th>Low-power mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_{PU2}$</td>
<td>$C_6 - 2/3 \cdot (C_3 + C_4)$</td>
<td>$C_6 - C_3$</td>
</tr>
<tr>
<td>$M_{PU1}$</td>
<td>$\frac{2}{3} \cdot (C_3 + C_4) - \frac{5}{6} \cdot (C_0 + C_1)$</td>
<td>$C_3 - C_0$</td>
</tr>
<tr>
<td>$M_{PU0}$</td>
<td>$\frac{5}{6} \cdot (C_0 + C_1)$</td>
<td>$0$</td>
</tr>
<tr>
<td>$M_{PD1}$</td>
<td>$C_5$</td>
<td>$0$</td>
</tr>
<tr>
<td>$M_{PD0}$</td>
<td>$C_2 - C_5$</td>
<td>$0$</td>
</tr>
</tbody>
</table>

**V. MEASUREMENT RESULTS**

Fig. 12 shows the measurement setup and a microphotograph of the prototype TX, which was fabricated in a 65-nm CMOS process and occupies 0.0333 mm$^2$. For testing purposes, the comparators and counters for the ZQ calibration are replaced by an inter-integrated circuit (I2C) and external comparison. The channel used for test has a 4.3-dB loss at 7 GHz. A chip on board (COB) is used for testing, which allows the measurement to focus on on-chip performance. The DQ node has the total $C_{IO}$ of approximately 300 fF, which includes the pad capacitance of about 100 fF. The output pad provides an electro-static discharge (ESD) protection up to 1-kV human-body model and 250-V charge-device model (CDM). The actual memory interfaces may have a relatively larger parasitic load due to more robust ESD protection and longer routing, which can lead to performance differences from our measurements. The eye diagrams of the output signal are measured by an oscilloscope with its internal termination. Even if the variation in the RX termination is included, the ZQ calibration can compensate for the variation and obtain the correct strength of each PU and PD drivers.

Table IV shows the measurement results of three-point calibration and these values are applied to the driver for the rest of the measurements. The ratio level separation mismatches (RLMs) are measured with both one-point calibration and three-point calibration, as shown in Fig. 13. Using one-point calibration, the measured RLM is 0.783, which can
TABLE IV
CALIBRATION RESULTS THROUGH MEASUREMENT

<table>
<thead>
<tr>
<th>Device (W/L)</th>
<th>Normal operation</th>
<th>Low-power mode</th>
</tr>
</thead>
<tbody>
<tr>
<td>$M_{PU2}$</td>
<td>3.2um / 60nm</td>
<td>5.6um / 60nm</td>
</tr>
<tr>
<td>$M_{PU1}$</td>
<td>3.6um / 60nm</td>
<td>3.2um / 60nm</td>
</tr>
<tr>
<td>$M_{PU0}$</td>
<td>4.4um / 60nm</td>
<td>2.4um / 60nm</td>
</tr>
<tr>
<td>$M_{PD1}$</td>
<td>2.1um / 60nm</td>
<td>Turned off</td>
</tr>
<tr>
<td>$M_{PD0}$</td>
<td>2.7um / 60nm</td>
<td>Turned off</td>
</tr>
</tbody>
</table>

partially be attributed to the resistorless driver structure. Using three-point calibration, the measured RLM is 0.993.

Fig. 14 shows the eye diagrams measured using a PRBS-7 pattern without a channel. During normal operation, the worst eye has a width of 31.5 ps and a height of 63.2 mV at 28 Gb/s, as shown in Fig. 14(a). In the low-power mode, the worst eye has a width of 37.2 ps and a height of 51.3 mV at 24 Gb/s, as shown in Fig. 14(b). Fig. 15 presents the eye diagram measured using four clock patterns, 8’b00001111, 8’b00111100, 8’b11110000, and 8’b11000011, at 28 Gb/s. Since the TX uses only the rising edges of the four-phase clocks, the result shows the four-phase characteristics. The measured intervals between each phase are 70.8, 71.4, 75.7, and 67.8 ps. Fig. 16 shows the eye diagrams measured using PRBS-15 and PRBS-31 patterns at 28 Gb/s. Only small performance degradation is shown compared with those when using a PRBS-7 pattern. The worst eye has a width of 30.9 ps and a height of 59.2 mV when a PRBS-15 pattern is applied and has a width of 30.3 ps and a height of 56.0 mV when a PRBS-31 pattern is applied. Fig. 17 shows the eye diagrams measured with a PRBS-7 pattern at 28 Gb/s during normal operation with the channel. Without FFE, the worst eye has no opening; but with symmetric FFE, the eye has a width of 13.8 ps and a height of 15.9 mV, as shown in Fig. 17(a) and (b). With asymmetric FFE, the worst eye has a width of 23.1 ps and a height of 35.1 mV, as shown in Fig. 17(c). The eye width is 67% greater and the eye height is 121% greater than that with symmetric FFE.

The bathtubs are measured with a signal quality analyzer for data validity for our TX, as shown in Fig. 18. The measurements are made for the three eyes of PAM-4 without the channel and equalization. The data patterns used are calculated in advance for each eye and applied to the signal quality analyzer. Bathtub curves are constructed corresponding to the upper, middle, and lower eyes, which have a common horizontal margin for a bit error rate (BER) of $10^{-12}$ of 0.16-UI using...
PAM-4 TX achieves a data rate of 28 Gb/s/pin and a pin efficiency of 200% with a lower clock frequency than other memory TXs. Our TX achieves an RLM of 0.993 without the use of resistors or inductors while satisfying both impedance matching and high linearity as a result of our proposed three-point ZQ calibration scheme. Its measured power consumption is 17.89 mW at 28 Gb/s, and its energy efficiency is 0.64 pJ/bit.

### VI. Conclusion

We have presented a 28-Gb/s/pin single-ended PAM-4 TX for memory interfaces. High linearity of PAM-4 signal and impedance matching are simultaneously achieved by an auxiliary PU driver in the proposed driver. The VM driver and the asymmetric FFE driver each have an NMOS-only structure which eliminates resistors and inductors, and therefore occupies a small area. The absence of resistors and inductors also makes this architecture well-suited for advanced CMOS technologies since resistors and inductors are not scaled with technology. A three-point PAM-4 ZQ calibration scheme compensates for impedance variation in both the TX driver and the RX termination at PAM-4 output levels. Our TX achieves a data rate of 28 Gb/s/pin, an RLM of 0.993, and an energy efficiency of 0.64 pJ/bit.

### References


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