A 28-Gb/s/pin PAM-4 Single-Ended Transmitter with High-Linearity and Impedance-Matched Driver and 3-Point ZQ calibration for Memory Interfaces

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Abstract
This paper presents a single-ended transmitter (TX) with a voltage-mode (VM) PAM-4 driver. The proposed driver simultaneously satisfies impedance matching and linearity, and occupies a small area without resistors and inductors. A ZQ calibration scheme that automatically and precisely adjusts the PAM-4 driver is also addressed. The proposed calibration has three calibration points, which allow the driver to have high linearity by taking into account the impedance variations of the TX and the receiver (RX) according to the output levels. The prototype chip is fabricated in 65 nm CMOS process and occupies 0.0333 mm². The proposed TX achieves a data rate of 28 Gb/s/pin with the level separation mismatch ratio (RLM) of 0.993 while consuming 0.64 pJ/b.

Keywords: PAM-4 transmitter, impedance matching, linearity, memory interface, ZQ calibration.

Introduction
With the rapidly growing demand for high-bandwidth DRAM, multi-level signaling has emerged as one of the solutions to the next generation memory interfaces. In particular, PAM-4 signaling maintains on-chip circuit speed while doubling bandwidth under the same channel conditions. However, the two major challenges of PAM-4 TXs are impedance matching and linearity. Mismatched impedance with the channel causes reflections, and a nonlinear output reduces the vertical margin which is already smaller than that of NRZ signaling [1], both of which reduce signal integrity. Recent memory interfaces use a N-over-N driver [2], a VM and single-ended structure, without using resistors and inductors to reduce power consumption and area for NRZ signaling. However, this is not suitable for PAM-4 signaling due to large impedance variations of pull-up (PU) and pull-down (PD) drivers according to changes in output level. Previous VM PAM-4 drivers [3,4] incorporate series resistors to alleviate impedance variations, but these resistors require a significant increase in area without fully addressing either impedance mismatch or nonlinearity. The proposed impedance-matched PAM-4 (IM-PAM-4) driver achieves both impedance matching and high linearity by using an additional PU driver. The driver also occupies a small area due to the resistorless and inductorless structure. Therefore, high bandwidth is achieved with little burden on the memory systems. A ZQ calibration scheme for the PAM-4 TX is also proposed and achieves high accuracy by having three calibration points and considering the impedance variations in both the TX and the RX.

Transmitter Architecture
Fig. 1 shows the overall block diagram of the proposed PAM-4 TX. The clock path generates 4-phase clocks and a 32-bit PRBS generator is used to test the prototype. The 32-bit data is then transmitted to a DQ driver through a 32:8 serializer (SER), an encoder and 4:1 SERs. The encoder has a simple structure consisting of one stage of logic and is placed in front of the 4:1 SERs for signal integrity at high speeds. Asymmetric equalization is used in the DQ driver to mitigate nonlinear slew rates. The proposed IM-PAM-4 driver has three PU drivers and two PD drivers, and its operation with 4 levels of PAM-4 is shown in the Fig. 2.

The IM-PAM-4 driver satisfies both impedance matching and linearity. For impedance matching, the sum of the impedances of the on-state PU and PD drivers equals the characteristic impedance of the channel, Z₀. For linearity, the impedance ratio of the on-state PU and PD drivers to the RX termination equals the desired output level. The additional PU driver allows both of equations to be maintained at all levels of PAM-4; the strength of each driver is shown in Fig. 2. Since the total impedance of the PU drivers is Z₀ at the +3 level, the total size does not increase for the additional PU driver compared to the conventional structure with two PU and two PD drivers. Furthermore, when transitioning between the +2 and +1 levels, the conventional structure has switching noise, which is caused by one of the MSB and LSB drivers turning off and the other turning on. By sharing one PD driver between the +2 and +1 levels, the proposed driver largely eliminates this noise. The calculated strength of each PU and PD driver is automatically and precisely adjusted by the ZQ calibration, which is described in detail in the next section.

ZQ Calibration Architecture
Fig. 3 shows the block diagram and operation of the ZQ calibration. The ZQ calibration consists of a block that uses a ZQ pin and a replica driver similar to that used for NRZ signaling and a block using a DQ pin, which allows calculations that reflect variations of the RX termination actually used in the interface. Bidirectional memory systems use transistors with large variations for the RX termination, which affect the output level, so the RX variations must be taken into account to achieve high linearity. Two comparators are attached to the DQ pin which increase the I/O capacitive load (Cᵢₒ), but since the calibration operates at very low speed, the gain of the comparator is small enough that the increase in the Cᵢₒ is negligible. Unlike the previous 1-point impedance control loops [3,4], the calibration is operated at three different points, 1/6-VDDQ, 1/3-VDDQ and 1/2-VDDQ to compensate for impedances that vary with output levels. This 3-point calibration combined with the proposed driver architecture allows the driver to have matched impedance and linearity at all levels of PAM-4. In the block including the DQ driver, two loops operate sequentially at each point as shown in Fig. 3. The results from the first loops are calculated through the digital block and reflected by the PU driver when the second loop runs. This procedure can calculate the accurate strength of all PU and PD drivers automatically.

Measurement Results
The prototype chip is fabricated in 65 nm CMOS process. The microphotograph is shown in Fig. 4 and the total active area of the TX is 0.0333 mm². Fig. 4 shows the power dissipation measured at a data rate of 28 Gb/s with a VDD of 1V and a VDDQ of 0.6V. The total power consumption of the
TX is 17.89 mW and the proposed IM-PAM-4 driver consumes 1.78 mW. Fig. 5 shows the measured eye diagram with PRBS-7 pattern at 28 Gb/s with and without asymmetric FFE. With FFE, the eye has a width of 24.6 ps and a height of 37.6 mV as shown in Fig. 5(b). Fig. 6 shows measured RLMs with the conventional 1-point calibration and the proposed 3-point calibration. The eye diagram with the 1-point calibration has an RLM of 0.783; this degree of nonlinearity can be partially attributed to the resistorless driver structure. On the other hand, the eye diagram with the 3-point calibration has an RLM of 0.993 as shown in Fig. 6(b). The performance of the prototype chip is summarized and compared with that of other recent works in Table 1. By using PAM-4, a high pin efficiency of 200% is achieved with a low clock frequency compared to other memory TXs. The proposed TX achieves a data rate of 28 Gb/s/pin, a high RLM without the use of resistors and inductors, and uniquely satisfies both impedance matching and high linearity. The measured power consumption is 17.89 mW, and its energy efficiency is 0.64 pJ/b.

References

![Fig. 1. Block diagram of proposed PAM-4 transmitter.](image1.png)

![Fig. 2. Proposed PAM-4 driver and its operation according to 4 levels of PAM-4.](image2.png)

![Fig. 3. Block diagram of proposed ZQ calibration for PAM-4.](image3.png)

![Fig. 4. Chip microphotograph, TX layout and power breakdown.](image4.png)

![Fig. 5. Measured eye diagram with PRBS7 pattern at 28 Gb/s (a) without FFE and (b) with FFE.](image5.png)

![Fig. 6. Measured RLMs with (a) 1-point calibration and (b) 3-point calibration.](image6.png)