A Stereo Audio Delta-Sigma DAC with 40-kHz Bandwidth and 103-dB SNR

Han Yang, Jun Soo Cho, Yujin Park, Hyunjong Kim, and Suhwan Kim

Abstract—A wide-band and low-noise stereo delta-sigma (ΔΣ) digital-to-analog converter (DAC) for audio applications is proposed. A multi-bit quantizer with data-weighted averaging is used to reduce quantization noise and a half-band finite impulse response filter is designed to increase the speed of the ΔΣ modulator. A direct-charge-transfer switched-capacitor DAC and a track-and-hold circuit with a deglitch timing are used to improve the operating speed and the linearity of the audio DAC. The chip is fabricated with a 0.13-μm CMOS process, which uses the supply voltages of 1.2 V for the digital domain and 3.3 V for the analog domain. The experimental results show that our audio DAC achieves 40-kHz bandwidth, 103-dB A-weighted signal-to-noise ratio, and −85-dB total harmonic distortion and noise.

Index Terms—Digital-to-analog converter, low-noise, wide-band, delta-sigma modulator, switched-capacitor circuits

I. INTRODUCTION

Recently, as the market for artificial intelligent speakers has expanded and become popular, high-quality audio coder-decoder (CODEC) is required. The delta-sigma (ΔΣ) digital-to-analog converter (DAC), one of the key components of the CODEC, is essential for generating high-performance audio signals with a signal-to-noise ratio (SNR) over 100 dB [1-3]. An anti-aliasing filter (AAF) is needed to reduce out-of-band noise (OBN). A low-sampling rate requires a high-order steep filter. However, making the roll-off very steep can cause phase shift or resonant peaks. Sampling at higher frequencies allows the AAF to be implemented above the audible frequency range, thus alleviating filter design conditions. In other words, 96 kHz or 192 kHz sampling frequency is used for better sound quality [4, 5].

An audio ΔΣ DAC is composed of a digital front-end (DFE) and an analog output stage. The DFE consists of a frequency interpolation filter and a ΔΣ modulator. The digital input signal is up-sampled with an oversampling ratio (OSR) in the interpolation filter. And the ΔΣ modulator suppresses the quantization noise by noise-shaping. Multi-level modulation reduces the quantization noise more than 1-bit modulation [3, 6]. But it requires a dynamic element matching (DEM) such as data-weighted averaging (DWA) to suppress the nonlinearities caused by the mismatch among elements [7, 8]. Increasing the OSR also helps to achieve high SNR by spreading the quantization noise over a wider frequency band. However, this requires faster, more power-intensive digital processing which is costly.

The analog output stage consists of an internal DAC and a reconstruction low-pass filter (LPF). It produces an analog audible signal and filters OBN. There are two ways to implement: a current-steering [2, 3] and a switched-capacitor (SC) [9, 10]. The current-steering type has the advantages of low-power consumption and small area, but it is very sensitive to clock jitter. To achieve low-power consumption as well as the clock jitter insensitivity, a direct-charge-transfer SC DAC (DCT-SC DAC) [11, 12] is presented. However, if the output of the SC DAC is in non-return-to-zero (NRZ)
format, whose output is not reset periodically, inter-symbol interference (ISI) issues can occur. The ISI is caused by dynamic error sources such as incomplete output settling and remained charge at parasitic capacitances [6]. The internal DAC of return-to-zero (RZ) formatted output is less sensitive to the ISI, but there is another problem of reduced signal power and increased harmonic distortion when the output is applied directly to the LPF.

In this paper, we propose a 40-kHz bandwidth and 103-dB SNR audio DAC fabricated in the 0.13-μm CMOS process. To achieve these performances, a 64× interpolation filter and a 5th-order ΔΣ modulator with a 5-bit quantizer using a digital half-band finite impulse response (FIR) filter is designed in the DFE. The DCT-SC DAC with the optimal bias current analysis of the opamp enhances the operating speed. Also, the internal DAC with RZ-formatted output reduces the ISI. A track-and-hold (T/H) circuit with deglitch timing [13] also improves the signal power and the linearity.

The rest of this paper is organized as follows: Section II shows the architecture of our audio ΔΣ DAC system. In section III, proposed circuit and analysis are described. Section IV and V show the experimental results and conclusion.

II. ARCHITECTURE

Fig. 1 shows the block diagram of the proposed audio ΔΣ DAC which consists of the DFE and the analog output stage. In the DFE, the frequency of the 20-bit input signal is increased by the interpolation filter as inserting zero samples between the input data [16]. Then the digital FIR filter removes the aliases and smoothens the zero-padded data. The sampled input signal at 96 kHz is up-sampled by a factor of OSR which is 64 with 2 stages of cascaded FIR filters and a sample-and-hold register.

The in-band noise is suppressed by the oversampling and noise-shaping principle of the digital ΔΣ modulator. To expand the input signal bandwidth up to the 40 kHz, the sampling rate of the ΔΣ modulator f_s is set to 96 kHz. The operating clock of the ΔΣ modulator f_clk is 6.144 MHz with the OSR of 64. A 5-bit quantizer is used in our ΔΣ modulator to reduce the quantization noise, suppress the idle tones, and improve the stability of the ΔΣ modulation loop. The mismatch among the quantizers is averaged by DWA technique [7, 8], which scrambles the 30-bit output codes of the thermometer decoder.

The internal DAC converts the decoded and shuffled 30-bit digital thermometer codes into a continuous-amplitude signal. The DCT-SC DAC has advantages such as less sensitivity to clock jitter noise and element mismatches compared to the current-steering DAC [11, 12]. The output of the internal DAC is RZ format that is robust to the ISI [6]. As shown in Fig. 2(a), the NRZ format output can cause different outputs with the same
inputs due to the incomplete settling or memory effects. However, the RZ format output guarantees the same outputs for the same inputs by placing reset intervals on each input samples as shown in Fig. 2(b). It only causes a gain error, which can be easily corrected later.

The output of the internal DAC is sampled and applied to the reconstruction filter. The reconstruction filter is typically implemented as LPF. This can be implemented as off-chip [12, 13] or on-chip [10, 14]. If the continuous-time LPF is followed by the discrete-time SC internal DAC, the signal power is reduced by the periodic output reset of the internal DAC. This problem does not occur when the internal DAC is implemented by a continuous-time current-adjustment internal DAC. To overcome this problem without losing the SC circuit advantages such as good ISI and device matching characteristics, we added a T/H circuit with de-glitch timing between the internal DAC and the reconstruction LPF [15]. A Sallen-Key type filter realizes a 2nd-order LPF to suppress OBN over 40 kHz. The reduced quantization noise of the 5-bit quantizer and 64 OSR relaxes the LPF specifications. Two identical single-ended 2nd-order Sallen-Key filters are designed in each channel that can drive a 20-kΩ and 5-pF off-chip load.

III. CIRCUIT IMPLEMENTATION

1. Digital Front-end

Fig. 3(a) shows the frequency interpolation process of the 20-bit digital input signal which is sampled at \(f_s\) of 96 kHz. The interpolation filter consists of 2 stages of cascaded half-band FIR filters [17] and a sample-and-hold register. First, zeros are inserted between adjacent digital data of the input signal to generate a twice sampling frequency signal. As shown in Fig. 3(b), the generated signal is smoothened by the half-band FIR filter that removes imaginary components. Table 1 shows the specifications of the 1st and 2nd half-band FIR filters that are identical. The order of the half-band FIR filter is 144, but the calculation is performed 72 times using 36 coefficients. The quadruple sampling frequency signal after two stages of cascaded half-band FIR filters is applied to the sample-and-hold register at a 16 times upsampling rate. The final oversampled output data is then generated at a frequency of 64\(f_s\), which is 6.144 MHz.

Fig. 4 shows the architecture of the 5th-order digital ΔΣ modulator. The signal and noise transfer functions of the ΔΣ modulator pass the audio-band signal up to 40 kHz and move the quantization noise to the out-of-band. The coefficients, \(a_i\) to \(a_5\) and \(b_1\) are implemented by multipliers and the delay units in the integrators are realized by registers. The up-sampled signals are truncated by the 5-bit quantizers. To alleviate the

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**Table 1. Specifications of 1st/2nd half-band filters**

<table>
<thead>
<tr>
<th>Parameter</th>
<th>Value</th>
</tr>
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<tbody>
<tr>
<td>Order</td>
<td>144</td>
</tr>
<tr>
<td>Oversampling ratio</td>
<td>2</td>
</tr>
<tr>
<td>Passband ripple</td>
<td>(4 \times 10^3) dB</td>
</tr>
<tr>
<td>Stopband</td>
<td>0.546 (f_s)</td>
</tr>
<tr>
<td>Stopband attenuation</td>
<td>(-110) dB</td>
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</tbody>
</table>
distortion problems caused by element mismatches in the internal DAC, the 31-level thermometer code converted from 5-bit data is shuffled by the DWA. It selects the elements sequentially according to the input, which results in averaging the mismatch among elements of the internal DAC.

2. Analog Output Stage

Fig. 5 shows the fully-differential 31-level DCT-SC DAC design. The unit capacitors $C_{[29:0]}$ sampled at $V_{\text{REFP}}$ or $V_{\text{REFN}}$ depending on the digital inputs at $\Phi_1$, and are fed back at $\Phi_2$ to produce an analog output value. The total feedback capacitance at $\Phi_2$ is $(C_s + C_t)$ where the $C_t$ is a fixed feedback capacitor. Due to the nature of the SC circuit, the clock jitter has negligible effects on the internal DAC performance unless the edges of the non-overlapping clocks, $\Phi_1$ and $\Phi_2$, are not swapped. In the capacitor array, $\Phi_{10}$, whose falling edge is delayed from $\Phi_1$, is used for the bottom-plate sampling. Otherwise, any on-resistance mismatch among switches that turn on at $\Phi_{10}$ in the capacitor array can cause signal-dependent distortions due to charge injections or thermal noise unbalances. The thermometer-decoded and shuffled digital inputs from the DFE reduce the mismatch of $C_{[29:0]}$ and improve the linearity. By reusing the sampling capacitors as feedback capacitors, the power consumption to charge or discharge the feedback capacitors is decreased. The auto-zeroing switch between the opamp input and the output removes the offset and low-frequency flicker noise even if they vary with temperature change or aging. The size of capacitors is determined by the $kT/C$ noise contribution. The analog output voltage of the internal DAC is as follows:

$$V_{\text{OUT}} = \frac{1}{C_s + C_t} \sum_{n=0}^{29} D_{\text{IN}}[n] C_s (V_{\text{REFP}} - V_{\text{REFN}})$$

In our design, the sampling rate of the DCT-SC DAC is 6.144 MHz, which is multiplied by the OSR of 64 at the Nyquist sampling frequency of 96 kHz. The unit capacitance is 628 fF for both $C_s$ and $C_t$ so that their ratio becomes consistent against process variations. The total sampling capacitance is 18.8 pF provided by 30 unit capacitors, and the $C_t$ is 22.6 pF. $V_{\text{REFN}}$ is actually ground level and $V_{\text{REFP}}$ is 3.3 V that is the same as the analog supply voltage, and the differential output swing is 3.0 Vpp.
Fig. 6(a) depicts the differential folded-cascode operational transconductance amplifier (OTA) used in the internal DAC. The bias current $I_D$ of the OTA should be large enough to diminish the total harmonic distortion (THD) but should be small to minimize the overall chip power dissipation. Although the DCT-SC DAC is a power-efficient structure, we have further optimized the current consumption of the OTA. Fig. 6(b) shows the output settling time of the OTA that consists of slew region and linear settling region. The required bias current for the slew region is determined by load capacitance $C_L$, slewing voltage $V_{slew}$, and slewing time $t_{slew}$ as follows:

$$I_D = \frac{C_L \cdot V_{slew}}{t_{slew}} \quad (2)$$

The required bias current for the linear settling region is determined by load capacitance $C_L$, return factor $\beta$, target effective resolution $B$, total settling time $t_{set}$, and $g_{m}/I_D$ ratio $R$ as follows:

$$I_D = \frac{C_L}{R\beta(t_{set} - t_{slew}) - \ln\left(\frac{2^{-B}}{2}\right)} \quad (3)$$

From (3) and (4), $t_{slew}$ is calculated as follows:

$$t_{slew} = \frac{V_{slew}R\beta t_{set}}{-\ln\left(\frac{2^{-B}}{2}\right) + V_{slew}R\beta} \quad (4)$$

The optimal bias current $I_D$ of the OTA is then computed by substituting $t_{slew}$ into either (2) or (3).

The image components produced by the internal DAC are removed, and the audio output signal is generated by the 2nd-order Sallen-Key filter as shown in Fig. 7(a). The sampling capacitor $C_s$ is 6 pF to suppress the kT/C noise and the 3-dB bandwidth is 400 kHz to pass the input signal frequency up to 40 kHz. The filter is designed with a drivability of 20-kΩ and 5-pF load and a differential output swing of 3.0 $V_{pp}$. The quality factor is designed to be 0.5 considering little signal droop.

Since the internal DAC is an RZ type whose output is reset at $\Phi_1$, applying the output of the internal DAC directly to the LPF diminishes the signal power by 6 dB since it averages both the meaningful input signal and reset values. To overcome this problem, the T/H circuit is
inserted between the internal DAC and the LPF. As shown in Fig. 7(b), the output signal is improved by 6 dB when the T/H circuit is used compared to the case when the T/H circuit is not used.

There is another factor that degrades the linearity performance of the audio DAC. If $\Phi_2$ is used for the T/H sampling switch, output glitches occur because the reconstruction filter tracks the incompletely settled input signal as shown in Fig. 7(c). To solve this issue, deglitch timing clock $\Phi_3$ is used for the T/H circuit operation. The rising edge of $\Phi_3$ is later than $\Phi_2$ to wait until the output of the internal DAC is settled sufficiently. To ensure settling of more than 99% of the internal DAC output, $\Phi_3$ goes high after $\Phi_2$ goes high with a delay time $(t_{\text{slew}} + 5\tau)$, where $t_{\text{slew}}$ and $\tau$ are the slew time and the time constant of the internal DAC, respectively. The falling edge of $\Phi_3$ is slightly faster than that of $\Phi_2$ to ensure that the output of the internal DAC is not reset. The T/H circuit is designed to be either activated or bypassed to verify the validity of the circuit and the deglitch timing.

IV. EXPERIMENTAL RESULTS

Fig. 8 is a die micrograph fabricated in 0.13-μm CMOS process, and the chip has two identical channels for stereo audio signal processing with the active area of 2,230 μm × 1,600 μm. The DFE is synthesized into a single block for two channels. Fig. 9 is a test PCB board with the fabricated chip in the center. Fig. 10 and 11 shows the measurement setup. Digital input signals are applied to our audio DAC chip with the inter-IC sound (I2S) format. The analog output signals are connected to the audio analyzer through stereo balanced connectors. The measured in-band spectrum with $-12$-dBFS input signal is shown in Fig. 12. The fast Fourier transform (FFT) is performed with 16,384 points. The black-colored graph indicates the FFT spectrum of the proposed audio DAC using T/H circuit and deglitch timing. The gray-colored graph is the FFT spectrum when the output signal of the internal DAC is directly connected to the LPF bypassing the T/H circuit. Thanks to the T/H circuit and the deglitch timing, the signal
power is increased from $-18$ dBV to $-12$ dBV and the THD+N is reduced from $-69.7$ dB to $-84.9$ dB. Fig. 13 shows the measured THD+N performance when the input signal power is swept from $-100$ to 0 dBFS. Fig. 14 shows that the output signal amplitude varies within $\pm \, 0.6 \, \text{dB}$ as the input frequency changes from 20 to 45 kHz at the 96-kHz sampling rate. The proposed audio DAC achieves 103-dB A-weighted SNR at a 1-kHz input and consumes 41.4 mW per channel.

Table 2 summarizes the performance and compares with other stereo audio DACs that are fabricated in 0.13-μm CMOS process. The figure of merit (FOM) of the audio DAC is defined as $\text{FOM}_{\text{SNR}} = \text{SNR} \cdot \frac{\text{BW}}{\text{Power}}$ [18]. The total power consumption of our chip is larger than other studies in Table 2, but it is caused by the 2x higher bandwidth as you can see the $\text{FOM}_{\text{SNR}}$ is better than [10]. The higher FOM$_{\text{SNR}}$ of [14] is due to its low supply voltage which results in the smaller output swing than ours.

V. CONCLUSIONS

A wide-band and low-noise stereo ΔΣ DAC for audio application is proposed. To increase the input bandwidth, a half-band FIR filter is designed in the ΔΣ modulator. The 5th-order ΔΣ modulator with 5-bit quantizer is realized to improve SNR performance. In the analog output stage, power efficient DCT-SC DAC is used as an internal DAC and the optimum current consumption is analyzed considering the slew and the linear settling region. The T/H circuit with deglitch timing tracks the RZ-formatted output of the internal DAC well with negligible signal loss and harmonic distortions. The 2nd-order Sallen-Key filter is implemented as a reconstruction filter. The circuit is fabricated with 0.13-μm CMOS process which uses the supply voltage of 1.2

<table>
<thead>
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<th>Table 2. Performance summary and comparison</th>
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<tr>
<td>Process</td>
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<tr>
<td>Supply Voltage (V)</td>
</tr>
<tr>
<td>Bandwidth (Hz)</td>
</tr>
<tr>
<td>Sampling Frequency (kHz)</td>
</tr>
<tr>
<td>Operating Clock Frequency (MHz)</td>
</tr>
<tr>
<td>Output Swing ($V_{\text{ref}}$)</td>
</tr>
<tr>
<td>SNR (dB(A))</td>
</tr>
<tr>
<td>THD+N (dB)</td>
</tr>
<tr>
<td>Power Consumption (mW)</td>
</tr>
<tr>
<td>FOM$_{\text{SNR}}$</td>
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V and 3.3 V for digital and analog domain, respectively. The proposed circuit achieves 40-kHz input bandwidth, 103-dB A-weighted SNR, and −85-dB THD+N with a −12-dBFS input signal at 1 kHz.

REFERENCES


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