ABSTRACT

In this paper, we propose a footer voltage feedforward technique for wide fan-in dynamic gates to achieve high noise immunity while maintaining the delay and energy performance. Dynamic multiplexers designed and simulated in 90nm CMOS are used to demonstrate the effectiveness of the proposed design style.

I. INTRODUCTION

Dynamic domino logic circuits are often employed to realize wide fan-in logic gates in high performance microprocessors, digital signal processors, and other VLSI circuits. As an example, a dynamic multiplexer used in a register file is shown in Fig. 1. Although fast and compact, wide dynamic gates introduce additional power and dual-phase pipeline overheads. In addition, they suffer from reduced noise margins as the evaluate node in a dynamic gate is vulnerable to a number of charge-loss mechanisms [1]. Noise-margins in deep-submicron (DSM) circuits are even more severely impacted due to increased leakage currents and stronger interconnect parasitic effects [2]. Therefore, wide fan-in gates require design techniques for improving the noise tolerance to compensate for the cumulative leakage from the parallel evaluation paths.

Conventionally, feedback keepers have been used to increase the noise tolerance. However, wide fan-in gates in DSM require very strong keepers for acceptable noise margins. Fig. 2 demonstrates the impact of keeper upsizing on the power-delay-product (PDP) performance of 8-to-32-bit dynamic multiplexers designed in 90nm CMOS technology. Keeper ratio (K) is defined as the ratio of the average current drivability of the keeper transistor to that of a single evaluation path. It was however determined through simulations that the device ratio (Width_{PMOS}/Width_{NMOS}) required to deliver the same average current was smaller than the ratio of their mobilities (\mu_{NMOS}/\mu_{PMOS}) [4]. Unity Noise Gain (UNG) values, measured as in [5], are normalized with respect to the supply voltage. While increasing K improves the noise tolerance, this is at the cost of significant increase in the PDP.

Figure 1: Local bit-line (LBL) organization of a register file (RF) using a conventional n-bit dynamic multiplexer [3].

Figure 2: Power-delay-product (PDP) performance with keeper upsizing for 8-to-32-bit dynamic multiplexers. PDP values normalized to PDP of 8-bit multiplexer with K=0.1.
due to increased gate delay and contention. PDP increases by 2.6X-3.6X for a K variation between 0.1 and 1. Therefore, the large performance overhead of keeper upsizing makes it an unsuitable design style for high fan-in domino gates [6]. Other design techniques are based on employing a conditional feedback keeper [7], raising the source voltage of evaluation transistors [8] and using the stacking effect [5] to improve the noise immunity. However, these noise-tolerant techniques also incur performance penalties, as detailed in Section II.

In this paper, we propose a domino design technique based on feedforwarding the footer voltage from the bottom node of the evaluation network to achieve a high noise margin while still retaining the advantage in performance. The feedforward path improves the evaluation speed and allows a reduced voltage swing at the dynamic node with large capacitive load. Thus, high noise tolerance with reduced performance overheads can be achieved.

II. PREVIOUS WORKS

Domino techniques aimed at reducing the serious contention problem from strong keepers in wide dynamic gates can be broadly categorized into two groups: designs employing a conditional keeper where the keeper is disabled (or weakened) during the gate evaluation and designs that achieve high noise immunity without requiring strong keepers by raising the source voltage of the evaluation transistors either by modifying the pull-down network [8] or by using the stacking effect [5]. While the conditional keeper technique (Fig. 3) is effective in enhancing the noise tolerance against sub-threshold leakage noise, the gate is still susceptible to external input noise during the switching time window as the dynamic node is not adequately protected by the weak keeper. In addition, conditional keeper techniques are suitable only for gates located close to clock phase boundaries [7].

The diode-footed domino technique [5] was proposed to achieve high noise robustness against both deep submicron subthreshold leakage and input noise while avoiding the problems of conditional keeper domino. However, like other techniques based on raising the source voltage of the input transistors, the degradation in the speed of the gate is significant when compared to conventional designs.

Fig. 4 depicts a wide domino gate based on the diode-footed scheme. A transistor in diode configuration, MN1 in Fig.4, is added in series to the evaluation network to reduce the leakage from the evaluation network by the stacking effect. However, as stacking effect also increases the equivalent resistance of the pull-down path, a mirror transistor is employed to activate a slave discharging path to increase the evaluation speed. The evaluation waveforms of a dynamic multiplexer using the diode-footed scheme is shown in Fig. 5. It can be seen that the mirror node rises only to a value slightly less than VDD/2 (VDD, the supply voltage = 1.2V). Consequently, limited swing on the mirror node limits the overdrive of the transistors in the mirror network (MN1 and the mirror transistor MN2). Since the dynamic node in wide gates sees a high capacitance due to the large parasitic contribution from the evaluation network, it cannot be rapidly pulled down by transistors with limited overdrive.
This is corroborated by comparisons with a conventional multiplexer (fig. 6) which reveals that even though the improvement in noise immunity is significant, the best-delay performance achieved using a current mirror is still below that of a conventional domino gate with an upsized keeper ($K=1$). It must be noted that the mirror ratio ($M = \frac{\text{Width}_{MN2}}{\text{Width}_{MN1}}$) cannot be arbitrarily increased to improve the evaluation speed as the diffusion capacitance from the mirror transistor will eventually limit the performance. In addition, increasing $M$ also erodes the noise robustness of the circuit [5].

III. PROPOSED DOMINO LOGIC

In order to overcome the noise limitations of the conditional keeper scheme and the speed limitations of the diode-footed scheme, we propose the footer voltage feedforward domino (FVFD). An illustrative model of the FVFD gate is shown in Fig.

7. The FVFD scheme has no footer transistor but instead uses charge sharing between the top (main dynamic node, DYN1) and bottom (FOOT) nodes of the pull-down network to activate two parallel paths during evaluation: a slow path (PATH1) connecting the DYN1 with high parasitic capacitance (due to the wide pull-down network) to the output though a HI-skewed inverter (I1) and a fast feedforward path (PATH2) that uses the footer voltage to rapidly pull down a second dynamic node (DYN2) with small parasitic capacitance and which is also coupled to the output through a HI-skewed inverter (I2). Since the low-to-high swing on the node FOOT is limited, a LO-skewed inverter (I3) is used to generate a complete swing on DYN2. Limited swings on DYN1 and FOOT can cause DC power consumption in I1 and I3 and therefore they must be disabled after the output has transitioned high. So, while the feedforward path speeds up the domino gate, the noise immunity is improved due to the self-reverse bias effect [9] of the evaluation network caused by the positive potential on FOOT. Further, charge sharing and the use of two evaluation paths also allows DYN1, the high-capacitance dynamic node, to experience only limited voltage swings during evaluation and precharge phases while the second dynamic node, separated from the evaluation network, undergoes a complete rail-to-rail swing. This can possibly offset the power overhead from the increased number of transistors in the FVFD scheme and provide additional power savings.
respectively. The inverter structure formed by MP3, MP4, MN1 and MN2 represents the inverter I3 and I1, I2 are combined with a single NAND gate. MP1 and MP2 are the precharge transistors, while MP3 and MP4 are the keeper transistors for the dynamic nodes DYN1 and DYN2. Similar to the diode-footed scheme, the keeper transistors are minimum-sized as the self-reverse biasing effect in the evaluation network itself leads to high noise tolerance and obviates the need for an upsized keeper. The clocked transistor MN2 is added for two reasons. First, since at the start of precharge, FOOT is at an intermediate voltage level (Fig. 9), a DC path might exist through MP2 and MN1. MN2 cuts-off this DC path by turning-off at the start of precharge. Second, in absence of MN2, DYN2 can be easily disturbed, on account of its small capacitance, by any negative-going ground-bounce noise that might turn-on MN1. The addition of MN2 prevents an erroneous evaluation on the second dynamic node with small capacitance by a noise event in the ground network.

The waveforms in Fig. 9 provide a further understanding of the working of the FVFD gate. When the evaluation network is turned ‘on’ by a rising input, DYN1 falls and FOOT rises to an intermediate voltage level through charge sharing between the two nodes. This change in DYN1 is reflected at the output through one of the PMOS transistors in the NAND gate. Meanwhile, MN1 is turned ‘on’ by the voltage developed on the footer node (FOOT) and rapidly pulls down DYN2. The PMOS transistor in the NAND gate connected to DYN2 then completes the evaluation by quickly pulling up the output node. After the clock goes low, DYN1 and DYN2 are precharged high while FOOT is pulled down to zero by MN3 to prepare for the next evaluation cycle. Also, during precharge, all the inputs remain low to prevent any charge sharing.

It must be noted that FVFD gate requires an additional keeper transistor MN4 connected to the FOOT node and driven by DYN2. This helps to prevent any charge build-up on the FOOT node in a noisy environment where successive noise pulses during evaluation are a possibility. As can be seen in the noise response waveforms of the FVFD gate in Fig. 10, the FOOT node is pulled down to zero after a noise perturbation thus preventing a false evaluation by a subsequent noise event. Since MN4 is also minimum-sized like MP3 and MP4, the impact on the delay performance of the gate is minimal.
IV. SIMULATION RESULTS

Dynamic multiplexers having fan-ins of 8, 16, 32 and 64, implemented using a conventional footless domino scheme, diode-footed scheme and the FVFD technique are simulated in 1.2V 90nm CMOS technology at the worst-case leakage corner (fast NMOS, slow PMOS at 110°C). Each gate drives a FO4 inverter load and a 1GHz clock with 50% duty cycle is used. The output inverters, evaluation and precharge transistors are sized equally for all the three designs. During the evaluation of the delay and the power characteristics, only one pull-down path is activated which represents the worst-case condition [7]. To account for the overhead of clocked transistors, the power consumption of the local clock buffer was included in the power measurements. Power is measured and averaged over an active clock cycle (output switches) and an idle clock cycle (output does not switch). Noise measurements are done at the worst-case noise condition [7] with equal noise pulses at each of the select inputs of the multiplexer. Noise metrics used for comparison are Unity Noise Gain (UNG) margin [10], Average Noise Threshold Energy (ANTE) [11] and Energy normalized ANTE (EANTE) [11]. For UNG measurement, the noise pulse width is fixed at the approximate rise/fall time of a FO4 inverter in 90nm technology (≈50ps).

Iso-delay points are determined for comparing power and noise performance of the conventional domino gate (K=0.6) with the FVFD gate. On the other hand, the diode-footed gate is compared with the FVFD gate at iso-UNG points in terms of evaluation delay and average power. FVFD gate is compared separately with the conventional and diode-footed schemes because of the wide difference between the two schemes’ delay and noise performance (Fig. 6). The performance improvement of FVFD for different fan-ins is shown in Fig. 11. It is observed that for same delay performance as a conventional gate, FVFD gates show a UNG improvement of 25-to-34% and a power reduction of 22-to-41% for fan-ins ranging from 8 to 64. When compared with the diode-footed gate under conditions of similar noise robustness (iso-UNG), it shows a delay improvement of 16-to-28% and a power reduction of 10-to-14%.

The performance and noise metrics of 16-bit multiplexers implemented in the three design styles are summarized in Table 1. The FVFD gate shows an EANTE improvement of 81% over the conventional scheme indicating that the proposed scheme incurs a considerably smaller energy penalty in improving the noise immunity. The FVFD multiplexer also improves the PDP performance by 27% over the diode-footed scheme. Even though the diode-footed and the FVFD gates are designed for equal UNG margins (noise pulse width = 50ps), the former has slightly better ANTE and EANTE values due to its better noise immunity for wider noise pulses (noise pulse width > 150ps). This is however not a concern as in deep sub-micron, most noise pulses are narrow due to the sharp rise and fall times of all circuits [12]. It can thus be seen that the FVFD technique achieves high noise immunity and competitive delay performance while being energy efficient.

Figure 11: 8-to-64-bit dynamic multiplexer simulation results. Conventional and FVFD iso-delay curves for (a) UNG, and (b) Average Power. Diode-footed and FVFD iso-UNG curves for (c) Evaluation Delay, and (d) Average Power.
Table 1: Performance summary of 16-bit dynamic multiplexers. PDP values normalized to conventional 8-bit multiplexer with \(K=0.1\). UNG normalized to VDD.

<table>
<thead>
<tr>
<th></th>
<th>PDP ((V^2)-ps)</th>
<th>UNG ((V^2)-ps/fJ)</th>
<th>ANTE ((V^2)-ps)</th>
<th>EANTE ((V^2)-ps/fJ)</th>
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<tr>
<td>Iso-delay</td>
<td></td>
<td></td>
<td></td>
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<tr>
<td>Conventional</td>
<td>3.98</td>
<td>0.36</td>
<td>32</td>
<td>0.8</td>
</tr>
<tr>
<td>FVFD</td>
<td>3.11</td>
<td>0.46</td>
<td>40</td>
<td>1.45</td>
</tr>
<tr>
<td>Improvement</td>
<td>-22%</td>
<td>+28%</td>
<td>+25%</td>
<td>+81%</td>
</tr>
<tr>
<td>Iso-UNG</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Diode-footed</td>
<td>4.29</td>
<td>0.47</td>
<td>48</td>
<td>1.56</td>
</tr>
<tr>
<td>FVFD</td>
<td>3.14</td>
<td>0.47</td>
<td>41</td>
<td>1.47</td>
</tr>
<tr>
<td>Improvement</td>
<td>-27%</td>
<td>-14%</td>
<td>-6%</td>
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Robustness of the FVFD performance (PDP) is evaluated by running 1000-point Monte-Carlo simulations (Fig. 12). The variation in transistor parameters - drawn gate length, channel doping concentration and gate oxide thickness follow a Gaussian statistical distribution with a three-sigma (3\(\sigma\)) variation of 10\% [13] while the temperature is varied uniformly between 10\(^\circ\)-110\(^\circ\)C. In addition, a 10\% variation in power supply is also assumed. Favorable values of mean and standard deviation of the PDP distribution, inset in Fig. 12, indicates robustness of the FVFD design under PVT variations.

![Figure 12: PDP Distribution Curves for 16-bit multiplexers. (S.D. stands for Standard deviation of the distribution. Dotted vertical lines represent the mean.)](image)

V. CONCLUSION

We have proposed a footer voltage feedforward technique that utilizes charge sharing and two parallel evaluation paths to achieve robust noise performance without appreciable degradation in performance. Simulation results demonstrate that when compared with conventional and existing noise reduction techniques, the proposed design achieves an improved trade-off between noise immunity, delay and power consumption.

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REFERENCES